A Modified Four-Step Commutation to Suppress Common-Mode Voltage during Commutations in Open-end Winding Matrix Converter Drives

Rohit Baranwal, Kaushik Basu, Ashish Kumar Sahoo, Ned Mohan

***Abstract*—Open-end winding matrix converter drives provide a higher voltage transfer ratio and better output voltage quality with more voltage levels in the output voltage, compared to single matrix converter drives. Pulse Width Modulation (PWM) techniques have been developed for open-end winding drives to suppress switching common-mode voltage at load terminals. The switching of bi-directional switches in this converter requires a step by step control of individual IGBTs, known as four-step commutation. However, commutation can cause glitches in common-mode voltage, leading to circulating currents in the open-end winding load. These currents result in additional losses in the load. This paper presents an analysis of the common-mode voltage glitches during commutation process. A modified four-step commutation scheme is then presented that reduces these glitches, thus suppressing circulating currents in the load. Simulation and experimental results have been presented to verify the reduction in circulating currents when using the proposed modified four-step commutation technique.**

***Index Terms*—Matrix converter, Open-end winding drive, Common-mode voltage, Commutation, Circulating current, Space vector modulation**

I. Introduction

Pulse width modulated power electronic converters are commonly used in power transmission and electric drive systems, due to their capability of synthesizing voltages and currents of desired amplitude and frequency [1]. The most common of these is the back to back two level three-phase voltage source inverter. This two stage power conversion requires a bulky DC electrolytic capacitor leading to a reduction in reliability and power density. Matrix converters (MC) present a single stage solution to synthesize AC voltage of desired amplitude and frequency from AC input, thus doing away with the DC link capacitor.

A power electronic converter can produce switching frequency common-mode voltages (CMV) at the load terminals, which can lead to electromagnetic interference (EMI), shaft voltage buildup and bearing and ground currents [2]–[4]. CMV can be reduced using which involve common mode filters as presented in [5]–[8], or by using PWM strategies for common-mode voltage reduction or elimination [9]–[12]. However, these PWM strategies lead to a reduction in maximum voltage transfer ratio [11], [12]. Open-end winding drives utilize two converters, one converter connected to each end of an open-end winding load [13], [14]. These drives provide higher maximum voltage transfer ratio compared to a single converter drive. An added benefit is an increase in the number of levels in the output voltage, thus having lower total harmonic distortion (THD) in load voltage and current. Different topologies of open-end winding drives have been explored, which incorporate two level inverters [15], multilevel inverters [16]–[19] and matrix converters [20]. PWM strategies have also been proposed for open-end winding drives for common-mode voltage elimination [15], [20], [21].

However, due to non-idealities in the drive system, such as voltage drops across switches and dead time, there are short intervals for which the common-mode voltage is non-zero or is at a different value than the constant value it is to be held at [22]. In open-end winding drives with a common input source for both converters, the glitches cause circulating currents. These currents cause extra losses in the load and are therefore, undesirable. PWM techniques to reduce circulating currents in a dual two level converter drive have been presented in [23], [24], but produce switching CMV at load terminals. In [22], a dead band compensation technique presented in [25] for two level converters has been used to suppress the common-mode voltage glitches during dead time in an open-end winding two level inverter drive, while using the PWM technique in [15], which does not cause switching CMV at load terminals.

A simple dead time is used in a two level inverter for preventing short circuiting of the DC input source. A matrix converter however uses four-step commutation which requires load current direction sensing [26], [27]. This paper presents an analysis of CMV glitches occurring due to commutation in open-end winding matrix converter drive. Then, a modified four-step commutation process that suppresses these glitches is presented. The paper is organized in seven sections. After the introductory first section, the second section describes the dual MC drive and CMV expressions. Analysis of CMV glitches during commutation and the proposed strategy to mitigate it are presented in section III and IV respectively. It is validated with simulation results in section V and experimental results in Section VI and the paper concludes in the seventh section.

II. Dual Matrix Converter drive and Common-Mode Voltage elimination

An open-end winding dual matrix converter drive has two matrix converters, one on each end of the three-phase load. A diagram of this drive is given in Fig. 1. A matrix converter has a total of nine bidirectional switches (each switch is realized using two IGBTs, as shown in Fig. 1 for the switch cC consisting of IGBTs $cC1$ and $cC2$), forming three legs,

978-1-4673-7151-3/15/$31.00 ©2015 IEEE

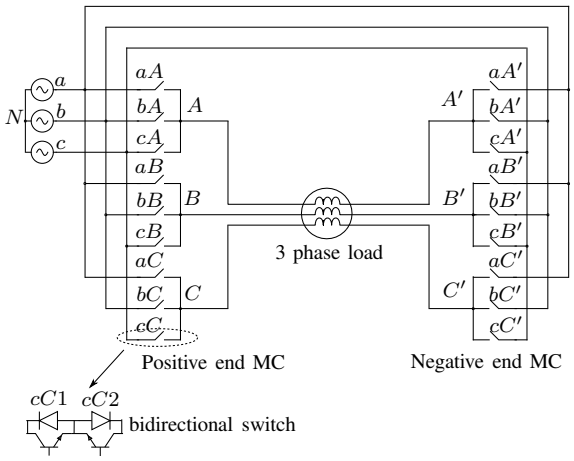


Fig. 1: Dual matrix converter drive

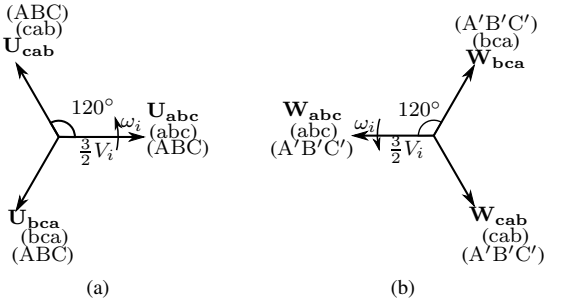


Fig. 2: CCW rotating vectors (a) Positive end (b) Negative end

one for each output phase. Each of the three output phases must be connected to any of the three input phases. Thus, a total of twenty-seven switching combinations are possible, each combination corresponding to a space vector [26].

Eighteen of these space vectors are stationary with time varying magnitude. Three vectors have zero magnitude and are called zero vectors. The remaining six vectors are constant in magnitude (equal to $1.5V_i$, where V_i is peak input phase voltage) and rotate at a constant speed and are known as synchronously rotating vectors. Three of these vectors rotate in counter clockwise direction at the input frequency ω_i and are known as counter clockwise or CCW vectors. The other three vectors rotate in clockwise direction at ω_i and are known as clockwise or CW vectors. The CCW vectors of the positive end converter are shown in Fig. 2(a). The CCW vectors of the negative end converter are shown in Fig. 2(b). They are opposite in direction to the CCW vectors of positive end converters, but are otherwise identical.

The positive end and negative end common-mode voltages are defined as the sum of instantaneous pole voltages at positive and negative ends of the load respectively, as written in (1).

$$v_{\mathrm{com,p}} = \frac{v_{AN} + v_{BN} + v_{CN}}{3}$$
$$v_{\mathrm{com,n}} = \frac{v_{A'N} + v_{B'N} + v_{C'N}}{3} \quad (1)$$

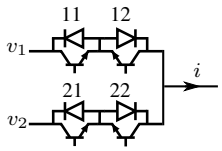


Fig. 3: Two bidirectional switches undergoing commutation

In case of CCW and CW vectors, each input phase is connected to only one output phase. Assuming that the input AC voltages are balanced, the common-mode voltage stays at zero on both positive and negative ends if only the synchronously rotating vectors are used for PWM of the open-end winding matrix converter drive [20].

III. Effect of Commutation process on Common-Mode Voltage

Real world power devices have finite turn ON and turn OFF times. Due to this, they can not be controlled with ideal PWM pulses. A commutation process is required for matrix converters to fulfill two conditions:

- No two phases of the input are ever short-circuited
- Output current is never interrupted

Conventional four-step commutation satisfies the above two requirements. The state machine of conventional four-step commutation is presented in Fig. 4. This state machine controls the switching of the individual IGBTs of two bidirectional switches shown in Fig. 3. In Fig. 3, v_1 and v_2 are the input voltages, while i is the load current. The states in Fig. 4 are denoted by alphabets A through H.

The quantities Q_{11}, Q_{12}, Q_{21} and Q_{22} when mentioned in the states in Fig. 4, denote that IGBTs 11, 12, 21 and 22 respectively are ON, in Fig. 3. When these quantities are not mentioned, the corresponding IGBT is OFF. For example, in state A in Fig. 4, Q_{11} and Q_{12} are mentioned which mean that IGBTs 11 and 12 in Fig. 3 are ON, while other IGBTs, i.e. 21 and 22 are OFF. The quantity δt represents one commutation step time in seconds and q_1 and q_2 are ideal pulses for the bidirectional switches in Fig. 3.

The conventional four-step commutation algorithm is described below. In the following discussion, the bidirectional switch to be turned ON is called the incoming switch, while the bidirectional switch to be turned OFF is called the outgoing switch.

- Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch
- Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt
- Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt
- Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt

In the above description, the active and passive IGBTs are decided by the load current direction.

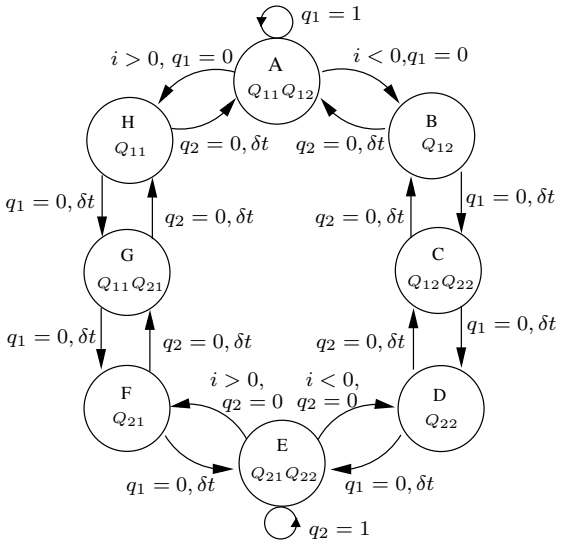


Fig. 4: Conventional four-step commutation state machine

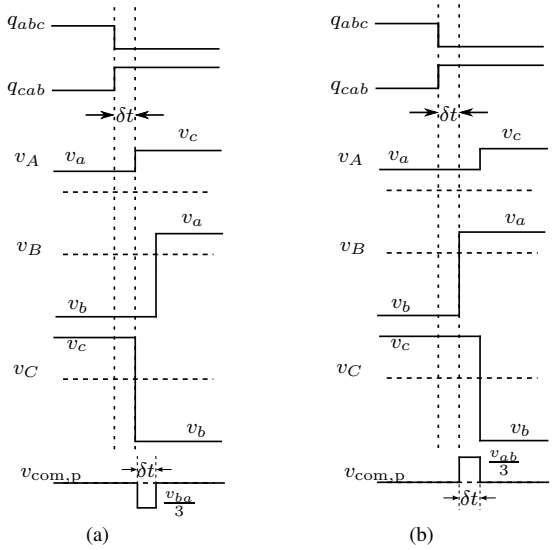


Fig. 5: Conventional commutation examples (a) Case 1 (b) Case 2

It has been mentioned in the previous section that the common-mode voltage can be kept at zero on both ends provided only synchronously rotating vectors are used for PWM. This happens since each input phase is connected to only one output phase, but this condition can be violated during commutation. For example, consider the case when the positive end converter in Fig. 1 is being switched from $\mathbf{U_{abc}}$ to $\mathbf{U_{cab}}$ and the current directions and voltage polarities are as given in Table I. The incoming (turning ON) and outgoing (turning OFF) bidirectional switches for each output phase of the positive end converter are given in Table II. The aforementioned four-step commutation algorithm is now applied to this example case, as described below for all three

TABLE I: Input voltage and load current polarities for example case 1

Parameter	v_{ab}	v_{bc}	v_{ca}	$i_{AA'}$	$i_{BB'}$	$i_{CC'}$
Sign	$+$	$-$	$+$	$+$	$-$	$-$

TABLE II: Incoming and outgoing negative end matrix converter switches for example case 1

Outgoing switch	aA	bB	cC
Incoming switch	cA	aB	bC

legs of the positive end matrix converter:

- Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch. Based on Table I and Table II, for output phase A, the IGBT $aA2$ is turned OFF. Similarly for output phase B and C, the IGBTs $bB1$ and $cC1$ are turned OFF, respectively.
- Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt. For output phase A, the IGBT $cA1$ is turned ON. Since voltage v_{ca} and current $i_{AA'}$ are positive, the commutation of load current $i_{AA'}$ happens naturally from $aA1$ to $cA1$. For output phase B, the IGBT $aB2$ is turned ON. The voltage v_{ab} is positive and current $i_{BB'}$ is negative, so the current keeps flowing through $bB2$ and commutation doesn't occur yet in phase B. For output phase C, the IGBT $bC2$ is turned ON. The voltage v_{bc} and current $i_{CC'}$ are negative, hence the current $i_{CC'}$ commutates naturally to IGBT $bC2$.
- Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. For output phase A, the IGBT $aA1$ is turned OFF. For output phase B, the IGBT $bB2$ is turned OFF. This causes the load current $i_{BB'}$ to commutate to IGBT $aB2$. For output phase C, the IGBT $cC2$ is turned OFF.
- Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt. For output phases A, B and C, the IGBTs $cA2$, $aB1$ and $bC1$ are turned ON respectively.

In the above steps, the commutation of load currents $i_{AA'}$ and $i_{CC'}$ is natural and happens in the second step of the four step process. However, the commutation of the load current $i_{BB'}$ is forced and takes place in the third step. This causes the input phase b to be connected to the output phases B and C together for one commutation step. Thus, the condition that each input phase is connected to only one output phase is violated for the period of one commutation step, leading to a non-zero common-mode voltage for that duration. The pole voltages v_A, v_B and v_C are shown in Fig. 5(a), displaying the glitch in CMV during four-step commutation. Thus, whenever there are two natural commutations and one forced commutation in the three output phases, there is a glitch in the common-mode

TABLE III: Conditions for Natural commutation

sgn(v_{12})	sgn(i)	Natural commutation
+	+	Yes
+	−	No
−	+	No
−	−	Yes

voltage.

In the above example, suppose the directions of the load currents are reversed (implying $i_{AA'} < 0$, $i_{BB'} > 0$ and $i_{CC'} > 0$), while keeping the input voltage polarities unchanged. Then the commutation of load currents $i_{AA'}$ and $i_{CC'}$ is forced, while the commutation of load current $i_{BB'}$ happens naturally. This causes the pole voltages of phase B to change one commutation step sooner than that of other two phases, as shown in Fig 5(b). Thus, the occurrence of two forced commutations and one natural commutation in the three output phases also results in a glitch in the common-mode voltage. As explained in [22], these glitches cause circulating currents in an open-end winding dual matrix converter drive, which are at the third harmonic of the fundamental output frequency.

IV. Modified Four-Step Commutation algorithm

In the conventional four-step algorithm, only the load current directions are used for the commutation process. It is seen from the analysis in the previous section, that the spikes in common-mode voltage occur due to a delay in the change in the pole voltage of a leg that is undergoing forced commutation in comparison with that of a leg undergoing natural commutation. Thus, the idea is to delay the natural commutation so that changes in all three output pole voltages occur simultaneously.

The conditions of natural commutation are identified in Fig. 3 and Table III. It is assumed that initially, IGBTs 11 and 12 are ON, while after the commutation process, IGBTs 21 and 22 are ON. The load current i is positive in the direction shown by the arrow in Fig. 3. In Table III, voltage $v_{12} = v_1 - v_2$. It is seen from the table that natural commutation occurs when the pole voltage is going up and output current is positive or when pole voltage is going down and output current is negative.

The state machine for modified four-step commutation is shown in Fig. 6(a). Similar to Fig. 4, the states in Fig. 6(a) are denoted by alphabets A through H. The quantities Q_{11}, Q_{12}, Q_{21} and Q_{22} when mentioned in Fig. 6(a), denote that the IGBTs 11, 12, 21 and 22 respectively are ON in Fig. 3. When these quantities are not mentioned, the corresponding IGBTs are OFF. For example, in state A in Fig. 6(a), Q_{11} and Q_{12} are mentioned, implying that IGBTs 11 and 12 in Fig. 3 are ON, while IGBTs 21 and 22 are OFF. The modified four-step commutation algorithm is described below.

1) Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch
2) If the condition of natural commutation is met, turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay of $2\delta t$, else turn ON the active IGBT after a delay of δt
3) Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay of δt
4) Turn ON the passive IGBT (whose anti-parallel diode will be conducting) of the incoming bidirectional switch

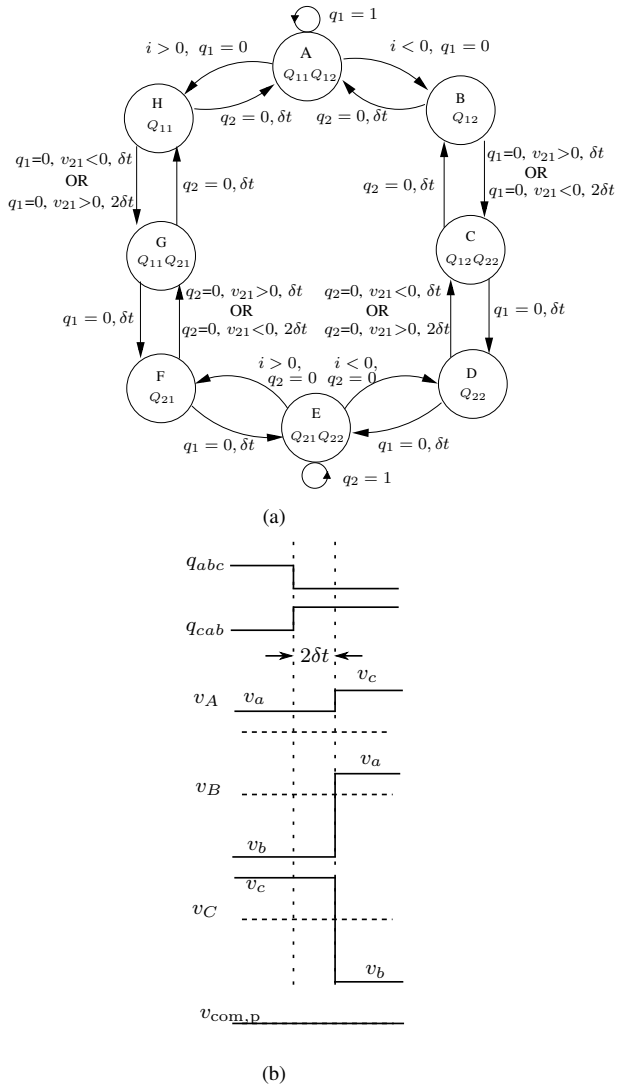


Fig. 6: (a) State machine diagram for proposed modified four-step commutation (b) Proposed four-step commutation example

The proposed modified four-step commutation process considers the polarity of voltage between incoming and outgoing bidirectional switches and output current direction and delays the second step of the four-step commutation process by one commutation step (δt) based on that. The delay is introduced when the condition of natural commutation is met. Delaying the second step by an additional δt when natural commutation occurs causes commutation in all phases of a matrix converter to occur together, irrespective of natural or forced nature

of the commutation. Thus, a glitch occurring in common-mode voltage due to the commutation process is suppressed by using the proposed modified four-step commutation. The first example discussed in previous section is described again below, this time using the modified commutation algorithm.

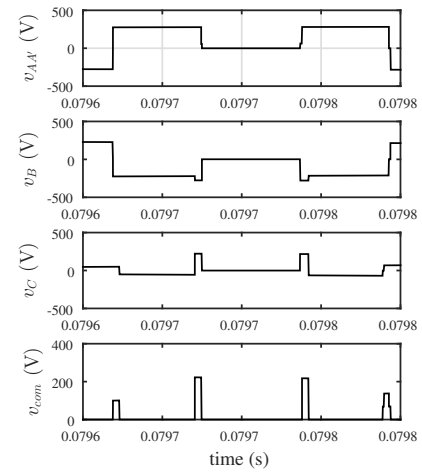
- Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch. Based on Table I and Table II, for output phase A, the IGBT $aA2$ is turned OFF. Similarly for output phase B and C, the IGBTs $bB1$ and $cC1$ are turned OFF, respectively.
- Step 2: Turn ON the active (which will be conducting) IGBT of the incoming bidirectional switch after a delay $2\delta t$ if natural commutation happens, else turn it ON after δt. For output phases A and C, natural commutaion happens. Hence, IGBTs $cA1$ and $bC2$ are turned ON after a delay of $2\delta t$. Thus, the voltage transition in these two phases happens at a delay of $2\delta t$ after the first step. In phase B, natural commutation doesn't happen, so IGBT $aB2$ is turned ON after a delay of δt. The voltage has not yet changed in phase B.
- Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. For output phase A, the IGBT $aA1$ is turned OFF. For output phase B, the IGBT $bB2$ is turned OFF. This causes the load current $i_{BB'}$ to commutate to IGBT $aB2$, thus causing the voltage transition in phase B to happen after a delay of $2\delta t$ from the first step. Thus, the voltage transition in all three load phases happens $2\delta t$ after the first step. For output phase C, the IGBT $cC2$ is turned OFF.
- Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt. For output phases A, B and C, the IGBTs $cA2$, $aB1$ and $bC1$are turned ON respectively.

As described above, the voltage transition in all three load phases happens $2\delta t$ after the commutation process begins, thus removing the glitch from the common mode voltage. This is illustrated in Fig. 6(b).

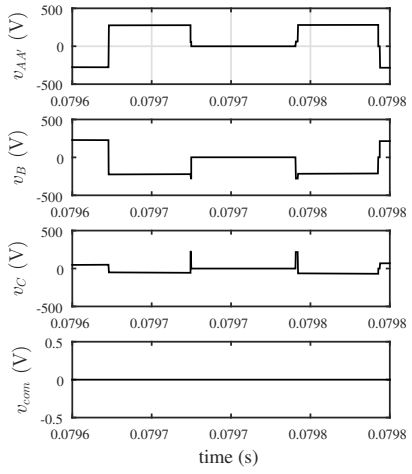
It should be noted, that input voltage sensing is already required for space vector modulation of a matrix converter. Thus, no additional components are required by the proposed commutation process. The state machine in Fig. 6(a) corresponds to the commutation between two bidirectional switches. But, it can be expanded to apply to three bidirectional switches for a three-phase to three-phase matrix converter.

V. Simulation results

A simulation of a dual matrix converter with the conventional four-step commutation and proposed modified four-step commutation has been done using MATLAB Simulink and the results have been presented for comparison. The simulation was done with 208 V line-line input rms voltage at 60 Hz and 135 V line-line output rms voltage at 15 Hz. The load is 50 kW at 0.8 power factor. The four-step commutation step δt is kept at 4 μs. The switching frequency is kept at 5 kHz.



(a)



(b)

Fig. 7: Simulation results (a) Load voltages and common-mode voltage for one carrier cycle, using conventional four-step commutation (b) Load voltages and common-mode voltage for one carrier cycle, using modified four-step commutation

In Fig. 7(a), the voltages across the three output phases and the common mode voltage across the load are shown for one switching period, when using conventional four-step commutation. The same have been shown in Fig. 7(b) when using modified four-step commutation. Common mode voltage spikes are visible in Fig. 7(a) due to voltage transitions not happening at the same time(as discussed in section III), whereas they are eliminated when using the modified four-step commutation, as observed in Fig. 7(b) (as discussed in section IV).

The three phase load currents and the frequency spectrum of load current in one phase are shown in Fig. 8(a) and Fig. 8(b) when using conventional and modified four-step commutation algorithms respectively. It is observed that the third harmonic component seen in Fig. 8(a) is nearly eliminated in Fig. 8(b).

Finally, plots of circulating current and its frequency response are shown in Fig. 9(a) and Fig. 9(b) when using conventional and modified -four step commutation algorithms respectively. The reduction of the circulating current when using modified four-step commutation is clearly visible both in the time domain plots and in the frequency spectra.

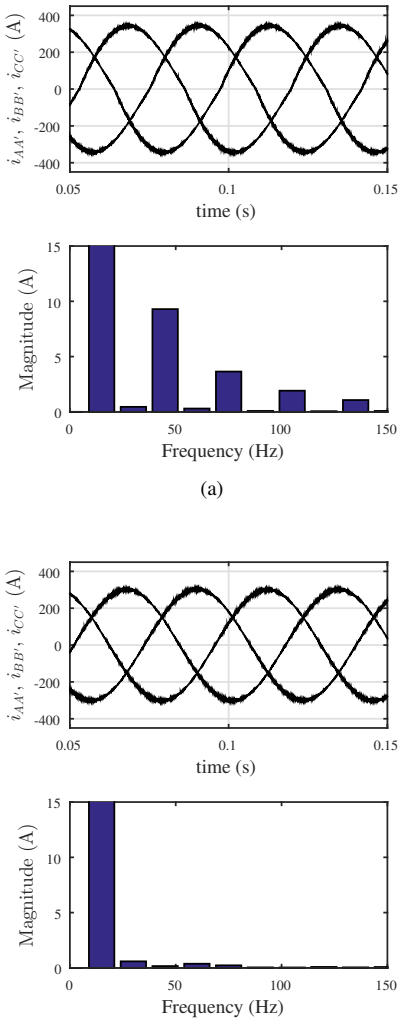


Fig. 8: Simulation results (a) Three-phase load currents and Fourier spectrum of one load current, using conventional four-step commutation (b) Three-phase load currents and Fourier spectrum of one load current, using modified four-step commutation

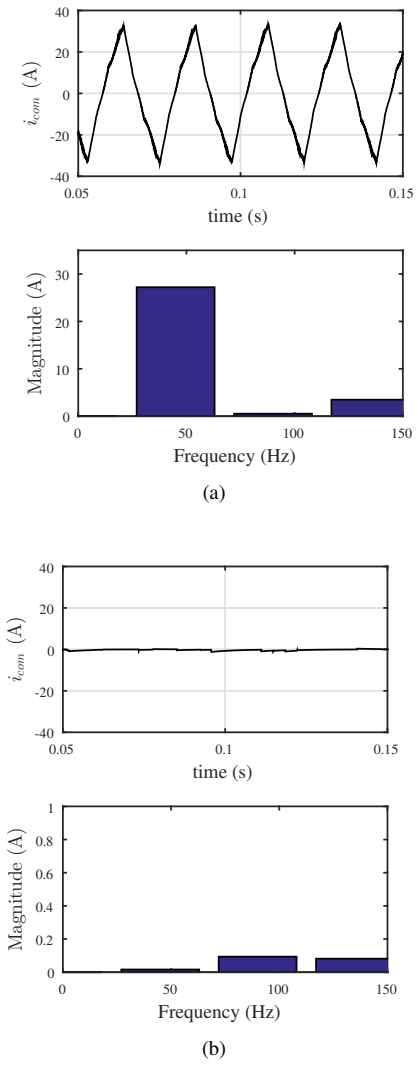


Fig. 9: Simulation results (a) Circulating current through the load and its Fourier spectrum, using conventional four-step commutation (b) Circulating current through the load and its Fourier spectrum, using modified four-step commutation

VI. Experimental results

The proposed modified four-step commutation and conventional four-step commutation have been implemented on a dual matrix converter drive. The hardware setup diagram is shown in Fig. 10. The matrix converter drive was built using Microsemi APTGT75TDU120PG IGBT modules and Concept 2SD106AI gate drivers. The electric motor used in the drive was a Baldor ZDM3581T, which is a 1 HP, 4 pole induction machine. The filter components used are R_d = 12.5 Ω, L_f = 1.4 mH and C_f = 35 μF. The output voltage across the machine was 36.7 V line-line rms at 12 Hz output frequency, while the input voltage was 86 V line-line rms at 60 Hz. The commutation interval δt was kept at 4.5 μs, while the switching frequency was 5kHz.

The voltages across the three output phases and the common mode voltage across the load are shown for one switching period in Fig. 11(a) and Fig. 11(b). It is seen that glitches appear in common-mode voltage in Fig. 11(a) (where conventional four-step commutation is used), as explained in section III and these glitches are nearly eliminated in Fig. 11(b) when using modified four-step commutation. The three-phase load

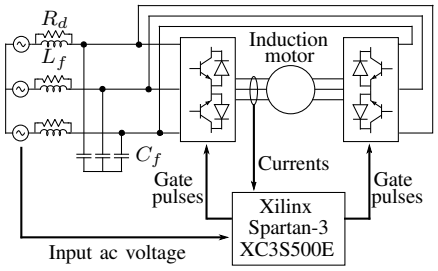
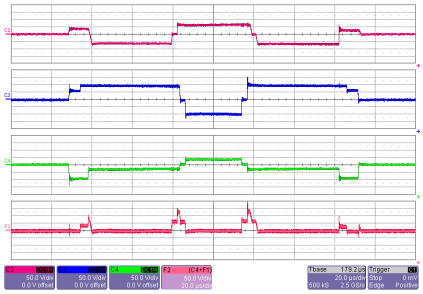
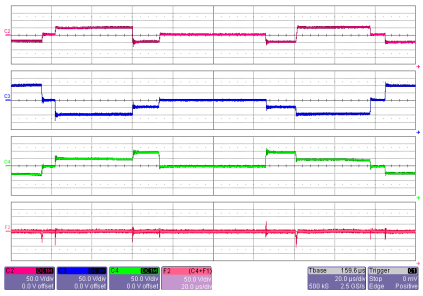


Fig. 10: Hardware setup diagram

currents and frequency spectrum of one load current are shown in Fig. 12(a) and Fig. 12(b). When using conventional four-step commutation as seen in Fig. 12(a), the magnitude of the third harmonic, which is at 36 Hz is seen to be nearly equal to 0.62 A. When the same results are taken using the modified commutation as seen in Fig. 12(b), the third harmonic reduces to 0.2 A. The circulating current and its frequency spectrum have been shown in Fig. 13(a) when using conventional four-step commutation and in Fig. 13(b) when using modified four-step commutation. It is seen that the magnitude of the fundamental component of the circulating current (at 36 Hz) goes from 1.77 A to 0.52 A when using modified four-step commutation.

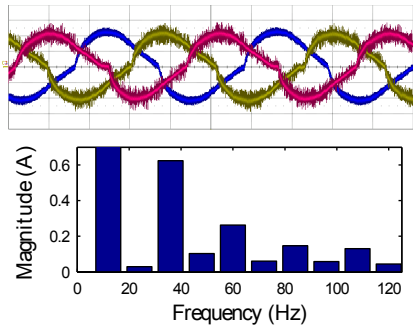


(a)

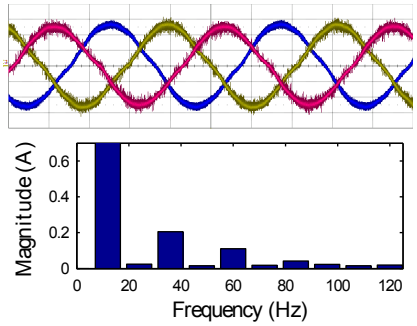


(b)

Fig. 11: Experimental results (a) Load voltages and common-mode voltage for one carrier cycle, using conventional four step commutation [X-axis: 20 μs/div, Y-axis: 50 V/div] (b) Load voltages and common-mode voltage for one carrier cycle, using modified four step commutation [X-axis: 20 μs/div, Y-axis: 50 V/div]



(a)



(b)

Fig. 12: Experimental results (a) Three-phase load currents and Fourier spectrum of one load current, using conventional four step commutation [For load current graphs: X-axis - 20ms/div, Y-axis - 2A/div] (b) Three-phase load currents and Fourier spectrum of one load current, using modified four step commutation [For load current graphs: X-axis - 20ms/div, Y-axis - 2A/div]

VII. Conclusion

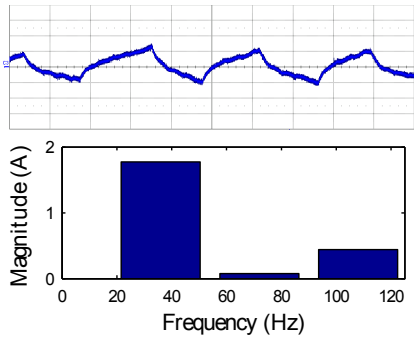
In the paper, the cause behind the glitches in common-mode voltage and resulting circulating currents due to four-step commutation has been studied. A modified four-step commutation process is then presented to reduce the glitches in the common-mode voltage, therefore minimizing circulating currents in the open-end winding load due to the commutation process. The proposed commutation technique requires additional information of the sign of the input line to line voltages. Finally, the presented simulation and experimental results successfully verify the effects of the modified four-step commutation process.

References

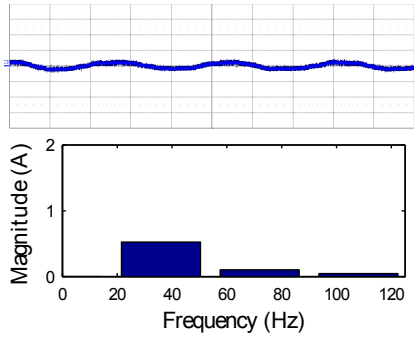
[1] J. Kolar, T. Friedli, J. Rodriguez, and P. Wheeler, "Review of three-phase pwm ac-ac converter topologies," *Industrial Electronics, IEEE Transactions on*, vol. 58, no. 11, pp. 4988–5006, Nov 2011.

[2] S. Chen, T. Lipo, and D. Fitzgerald, "Source of induction motor bearing currents caused by pwm inverters," *Energy Conversion, IEEE Transactions on*, vol. 11, no. 1, pp. 25 –32, mar 1996.

[3] S. Chen, T. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in pwm inverter drives," *Industry Applications, IEEE Transactions on*, vol. 32, no. 6, pp. 1365–1370, 1996.



(a)



(b)

Fig. 13: Experimental results (a) Circulating current through the load and its Fourier spectrum, using conventional four step commutation [For circulating current graphs: X-axis - 10ms/div, Y-axis - 2A/div] (b) Circulating current through the load and its Fourier spectrum, using modified four step commutation [For circulating current graphs: X-axis - 10ms/div, Y-axis - 2A/div]

[4] J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Effect of pwm inverters on ac motor bearing currents and shaft voltages," *Industry Applications, IEEE Transactions on*, vol. 32, no. 2, pp. 250 –259, mar/apr 1996.

[5] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *Industry Applications, IEEE Transactions on*, vol. 28, no. 4, pp. 858–863, Jul 1992.

[6] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a pwm inverter," *Power Electronics, IEEE Transactions on*, vol. 13, no. 5, pp. 835–841, Sep 1998.

[7] H. Akagi and S. Tamura, "A passive emi filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *Power Electronics, IEEE Transactions on*, vol. 21, no. 5, pp. 1459–1469, Sept 2006.

[8] H. Akagi and T. Doumoto, "An approach to eliminating high-frequency shaft voltage and ground leakage current from an inverter-driven motor," *Industry Applications, IEEE Transactions on*, vol. 40, no. 4, pp. 1162–1169, July 2004.

[9] K. Tian, J. Wang, B. Wu, D. Xu, Z. Cheng, and N. Zargari, "A new space vector modulation technique for the reduction of common-mode voltages in both magnitude and third-order component," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[10] A. Hava and E. Un, "A high-performance pwm algorithm for common-mode voltage reduction in three-phase voltage source inverters," *Power Electronics, IEEE Transactions on*, vol. 26, no. 7, pp. 1998–2008, July 2011.

[11] A. Ruderman and B. Reznikov, "Evaluation of motor pwm loss increase due to zero common-mode voltage modulation strategy of multilevel converter," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International*, 2010, pp. T3–66–T3–72.

[12] H.-N. Nguyen and H.-H. Lee, "An enhanced svm method to drive matrix converters for zero common-mode voltage," *Power Electronics, IEEE Transactions on*, vol. 30, no. 4, pp. 1788–1792, April 2015.

[13] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Power Electronics and Applications, 1993., Fifth European Conference on*, 1993, pp. 7–14 vol.5.

[14] T. Kawabata, E. Ejiogu, Y. Kawabata, and K. Nishiyama, "New open-winding configurations for high-power inverters," in *Industrial Electronics, 1997. ISIE '97., Proceedings of the IEEE International Symposium on*, vol. 2, 1997, pp. 457–462 vol.2.

[15] M. R. Baiju, K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *Power Electronics, IEEE Transactions on*, vol. 19, no. 3, pp. 794–805, 2004.

[16] P. Tekwani, R. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and dc-link capacitor voltage balancing using only the switching-state redundancy 2014;part i," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 5, pp. 2600–2608, Oct 2007.

[17] P. Tekwani, R. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and dc-link capacitor voltage balancing using only the switching-state redundancy 2014;part ii," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 5, pp. 2609–2617, Oct 2007.

[18] G. Mondal, K. Sivakumar, R. Ramchand, K. Gopakumar, and E. Levi, "A dual seven-level inverter supply for an open-end winding induction motor drive," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 5, pp. 1665–1673, May 2009.

[19] G. Mondal, K. Gopakumar, P. Tekwani, and E. Levi, "A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 4, pp. 2344–2351, Aug 2007.

[20] R. Gupta, K. Mohapatra, A. Somani, and N. Mohan, "Direct-matrix-converter-based drive for a three-phase open-end-winding ac machine with advanced features," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 12, pp. 4032–4042, 2010.

[21] H.-D. Lee and S.-K. Sul, "Common-mode voltage reduction method modifying the distribution of zero-voltage vector in pwm converter/inverter system," *Industry Applications, IEEE Transactions on*, vol. 37, no. 6, pp. 1732–1738, Nov 2001.

[22] A. Somani, R. Gupta, K. Mohapatra, and N. Mohan, "On the causes of circulating currents in pwm drives with open-end winding ac machines," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 9, pp. 3670–3678, 2013.

[23] V. Somasekhar, S. Srinivas, and K. Kumar, "Effect of zero-vector placement in a dual-inverter fed open-end winding induction-motor drive with a decoupled space-vector pwm strategy," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 6, pp. 2497–2505, June 2008.

[24] V. Somasekhar, S. Srinivas, B. Prakash Reddy, C. Nagarjuna Reddy, and K. Sivakumar, "Pulse width-modulated switching strategy for the dynamic balancing of zero-sequence current for a dual-inverter fed open-end winding induction motor drive," *Electric Power Applications, IET*, vol. 1, no. 4, pp. 591–600, July 2007.

[25] D. Leggate and R. Kerkman, "Pulse-based dead-time compensator for pwm voltage inverters," *Industrial Electronics, IEEE Transactions on*, vol. 44, no. 2, pp. 191–197, Apr 1997.

[26] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 2, pp. 276–288, Apr 2002.

[27] L. Herrero, S. de Pablo, F. Martin, J. Ruiz, J. Gonzalez, and A. Rey, "Comparative analysis of the techniques of current commutation in matrix converters," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, June 2007, pp. 521–526.